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As a below named translator, I hereby declare that:

My residence, post office address and citizenship are as stated bellow next to my name.

I translated the Certified copy of the priority document of Korean Patent application No. 10-2003-0011683 filed February 25, 2003 for U.S. patent Application No. 10/776,600.

I hereby state that the English translation is true and accurate, and further that this translation was made with the knowledge.

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Translator's signature:

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ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device has a fuse device cut electrically without a breakage caused by using laser beam or current. The semiconductor integrated circuit device employs, as the fuse device for storing status information, a MOSFET of a single polysilicon EEPROM cell type manufactured through a process of a volatile semiconductor memory.

TITLE OF THE INVENTION

Semiconductor Integrated Circuit having Non-volatile Memory Cell Transistor fabricated by Volatile Semiconductor Memory Process as Fuse Device

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to a semiconductor integrated circuit device. More particularly, the present invention relates to a semiconductor integrated circuit device having as a fuse device a non-volatile memory cell transistor fabricated by a volatile semiconductor memory process.

2. DESCRIPTION OF THE RELATED ART

A semiconductor memory device is generally classified into a volatile semiconductor memory device and a non-volatile

semiconductor memory device. The volatile semiconductor memory device may be subdivided into a dynamic random access memory and a static random access memory. The volatile semiconductor memory device has a characteristic of losing contents stored at memory cells when an external power source supply is cut off. While, the non-volatile semiconductor memory device may be divided into a mask read only memory (MROM), a programmable read only memory (PROM), an erasable programmable read only memory (EPROM), and an electrically erasable programmable read only memory (EEPROM) etc.

Such kinds of non-volatile semiconductor memory devices can permanently preserve the contents stored at the memory cells even thought the external power source supply is cut off, thus the devices are usually used to store data to be preserved regardless of the supply of power source. However, general users are difficult to freely perform erase and write operations or programming operation in MROM, PROM and EPROM, by itself in an electronic system. That is, it is not easy to erase or re-program the programmed contents under an on-board state. Meanwhile, in the EEPROM, the erase and write operation can be electrically performed in the system itself, thus its application to a system program storage device or auxiliary memory device necessary for a consecutive contents update is being increased gradually.

In the meantime, a semiconductor integrated circuit

device having a volatile memory such as a DRAM(Dynamic Random Access Memory) and an SRAM(Static Random Access Memory) etc. has generally employed a fuse for a fault recovery (hereinafter, referred to as "fuse device") in a defect address storage circuit in order to relieve for an electric characteristic fault of a memory cell. A polysilicon fuse composed of polysilicon layer has been initially used as such a fuse device, and has been manufactured together in a formation process of a gate electrode of a MOS field effect transistor(FET) or a wiring layer.

The fuse device was generally cut by light source such as laser beam etc. The cutting using laser beam requires a process of a laser cutting working executed in a separate wafer or separate chip. Further, if polysilicon melted in the laser cutting working remains on the neighborhood of the cutting portion, it affects the fuse adjacent thereto or the cut fuse may operate like a re-connected fuse, which may drop reliability for a fuse trimming work.

To solve such a fuse cutting problem by laser beam, a fuse cutting method using a current blowing has been also used in this field as shown in FIG. 1.

Referring to FIG. 1, a resistance value of a fuse device F1 made of polysilicon layer is determined much lower than a resistance value of a fixed resistance R. Thus, at an initial mode when a source voltage EVCC is applied, an address signal

ADDR is applied as a low state, and an external drive signal MRS is applied as a high state; a logic level of a node A becomes "H" and a logic level of a node B becomes "L". At this time, a logic level of a redundancy enable signal PREi outputted from an output inverter IN2 becomes "L". Meanwhile, in case a defect memory cell should be repaired, the source voltage EVCC is applied and the address signal ADDR is provided as a high state. Thus, an N-type MOS transistor N1 for a fuse blowing is turned on, and then an over current through the fuse device F1 starts on flowing. That is, the fuse device F1 is broken by the over current flowing from the fuse device F1 to a source terminal of the N-type MOS transistor N1. If the fuse device F1 is blown by current, the source voltage EVCC can be not applied to a source of a P-type MOS transistor P1 regardless of a state of the address signal ADDR, but is applied only through a resistance R. Therefore, when the drive signal MRS is applied as a high state, a logic level of the node A becomes "L" and a logic level of the node B becomes "H". Thus, a logic level of the redundancy enable signal PREi is outputted as "H", to repair a defect memory cell as a redundancy memory cell. If a logic level of the redundancy enable signal PREi is "L", it indicates as an example that a defect address is not stored, and if "H", it indicates that the defect address is stored. In any other case, this can be realized by its opposite logic.

However, though the current blowing method referred to FIG. 1 has an advantage that the method can be used in a package state together with a wafer state, there are still problems that the fuse device is again connected after a breakage of the fuse device, or that layers neighboring to the fuse device are damaged by the breakage of the fuse.

To try to solve the breakage problem of the fuse device, it was provided a prior art for an N-channel MOSFET having a floating gate, as a fuse device in a volatile semiconductor memory field. In this prior art, a cutting operation of the transistor as the fuse device is performed by irradiating electron beam generated by an electron beam apparatus through an opening part of an isolation layer formed on an upper part of the floating gate. That is, when electron is injected into the floating gate, a threshold voltage of the N-channel MOSFET is varied, thus the transistor functions as a fuse having an electrically cut state.

However, in this art it is also accompanied a process of separately irradiating electron beam to the N-channel MOSFET to be programmed by using the electron beam apparatus, similarly to the cutting process using laser beam. That is, under the programmed state that the electron is injected into the floating gate through the irradiation of the electron beam, it is difficult to return to an original state, which is caused by the reasons why the N-channel MOSFET has no a

control gate which is equipped with a memory cell transistor of the EEPROM, and why program and erase operations can not be performed with an apply of voltage. It means that the N-channel MOSFET having the floating gate cannot perfectly perform an operation like the memory cell transistor of the EEPROM.

It is therefore required a technique capable of easily fabricating a non-volatile memory cell as a fuse device that can perform an operation like the memory cell transistor of the EEPROM, by using a fabrication process of a volatile semiconductor memory such as DRAM and SRAM etc.

However, a general non-volatile semiconductor memory, e.g., a memory cell transistor of EEPROM needs a high voltage, e.g., about 10 through 18 volt for a program voltage, and needs a read voltage of about 5 volt. Thus, a chip internally employs a high voltage pump circuit, and a memory cell transistor has a floating gate surrounded with a dielectric film and has a control gate formed on an upper part of the floating gate, differently from the general MOSFET. That is, a process of fabricating the non-volatile semiconductor memory is much different from a fabrication process of a volatile semiconductor memory. There are many difficulties to manufacture the memory cell transistor of EEPROM under the fabrication environment of the volatile semiconductor memory device such as DRAM etc. without an additional process or a

change of the process.

SUMMARY OF THE INVENTION

Accordingly, a feature of the present invention is to provide a fuse device of a volatile semiconductor memory device capable of solving problems of the prior art.

Another feature of the present invention is to provide a semiconductor integrated circuit device having as a fuse device a non-volatile memory cell transistor fabricated in a fabrication process of a volatile semiconductor memory.

Another feature of the present invention is to provide a fuse device electrically cut without a breakage caused by using laser beam or current.

Still another feature of the present invention is to provide a method of manufacturing a fuse device through a fabrication process of a volatile semiconductor memory, and a structure of the fuse device therefor, which is capable of operating like a memory cell transistor of EEPROM.

Another feature of the present invention is to provide a structure of a fuse device capable of performing an operation like a memory cell transistor of EEPROM at a voltage lower than an operating voltage of the EEPROM.

Yet another feature of the present invention is to provide a structure of an EEPROM memory cell transistor as a fuse device capable of performing an operation like the memory

cell transistor of the EEPROM within an operating voltage range of a volatile semiconductor memory.

Another feature of the present invention is to provide a non-volatile memory cell transistor of a single polysilicon structure in which a fuse device cut without a breakage after making under a DRAM fabrication environment can be repaired to an original state not cut only when necessary.

Another feature of the present invention is to provide a structure of an EEPROM memory cell transistor used as a fuse device, in case a fault bit address is stored or a mode entry signal indicating an entry into a specific operating mode such as a test mode etc. is stored.

An additional feature of the present invention is to provide a semiconductor integrated circuit device having a fuse device cut without a breakage and repaired even under a packaging state.

Another feature of the present invention is to provide a defect address storage circuit of a semiconductor integrated circuit device having as a fuse device a non-volatile memory cell transistor manufactured in a fabrication process of a volatile semiconductor memory.

To these ends, according to one aspect of the present invention, a semiconductor integrated circuit device uses a MOSFET of a single polysilicon EEPROM cell type manufactured by a volatile semiconductor memory fabrication process, as a

fuse device for storing status information.

The single polysilicon of the MOSFET corresponds to a charge storage floating gate of EEPROM, and a control gate of the EEPROM is spaced from a channel region of the MOSFET and can be composed of a second conductive ion-implantation region formed in a lower layer of the single polysilicon. The MOSFET can be an n-channel MOSFET, in which a program operation for electrically cutting the fuse device can be obtained by injecting electron into the floating gate through a hot electron injection method. Further, an erase operation for electrically connecting the fuse device can be performed by discharging electron captured by the floating gate through an F-N((Fowler-Nordheim) tunneling system.

According to another aspect of the present invention, a defect address storage circuit of a semiconductor integrated circuit device includes a MOSFET of a single polysilicon EEPROM cell type, an operation enabler and a latch.

The MOSFET of the single polysilicon EEPROM cell type functions as a fuse device for storing status information, for which a drain is connected to a first power source and a control gate is connected to a second power source. Further, the MOSFET is manufactured through a fabrication process of a volatile semiconductor memory.

The operation enabler connects a source of the MOSFET to a ground power in response to a state of an enable signal.

The latch latches, as the status information, a voltage level appearing in a source of the MOSFET according to a change of a threshold voltage of the MOSFET, in case a defect address is stored.

The MOSFET of the single polysilicon EEPROM cell type is manufactured by the fabrication process of a volatile semiconductor memory. The MOSFET is composed of a first conductive substrate; a second conductive deep well formed on one portion of the first conductive substrate; a first conductive pocket well formed within the second conductive deep well; source and drain formed as a second conductive ion-implantation region in a portion of the first conductive pocket well; a second conductive well formed on another portion of the first conductive substrate, being spaced from the second conductive deep well; a control gate formed as the second conductive ion-implantation region in a portion of the second conductive well; and a floating gate of polysilicon layer material extendedly formed till a partial upper part of the control gate, passing on upper parts of the first conductive pocket well and the second conductive deep well in a direction roughly right-angled to the source-drain channel, and interposing a tunnel oxide. Herewith, a program operation can be realized through grounding with a source of the MOSFET and through an apply of the first and second power source as each of about 3 and 5 volt.

Further, the erase operation is obtained, through a grounding or floating of the source of the MOSFET, and by applying the first and second power source as each of about 5 and 0 volt. The read operation is performed, through a floating of the source of the MOSFET and by applying all the first and second power source as about 3volt.

The operation enabler may be provided as an N-type MOS transistor, and the latch can be an inverter latch whose input terminals are connected with output terminals one another. An output inverter for inverting and outputting an output of the latch can be further equipped therewith.

Herewith, the second conductive type can be an n-type impurity if the first conductive type is a p-type impurity.

BRIEF DESCRIPTION OF THE DRAWING

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

FIG. 1 is a circuit diagram of a defect address storage circuit using a general current blowing method;

FIG. 2 is a circuit diagram of a defect address storage circuit according to an exemplary embodiment of the present invention;

FIG. 3 is a layout of a fuse device referred to FIG. 2, provided as a non-volatile memory cell transistor having a single polysilicon structure;

FIG. 4 is a sectional view of an X-X' line referred to FIG. 3; and

FIG. 5 is a graph illustrating a program operating characteristic of the fuse device shown in FIG. 2.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

Hereinafter, preferred embodiments of the present invention will be described in detail with reference to FIGS. 2 through 5 in which like components having like functions have been provided with like reference symbols and numerals.

It will be understood by those skilled in the art that the present invention can be embodied by numerous different types and is not limited to the following described embodiments. The following various embodiments are exemplary in nature.

A semiconductor integrated circuit device having, as a fuse device, a non-volatile memory cell transistor fabricated by a process of a volatile semiconductor memory will be described as follows.

FIG. 2 is a circuit diagram of a defect address storage circuit according to an exemplary embodiment of the present

invention. Referring to FIG. 2, the defect address storage circuit of a semiconductor integrated circuit device includes a fuse device MN1, an operation enabler MN2, a latch L1 and an output inverter IN3.

In the fuse device MN1, a drain is connected to a first power source VCC and a control gate is connected to a second power source IN1, so that the fuse device MN1 functions to store status information. The fuse device MN1 is provided as the MOSFET MN1 of a single polysilicon EEPROM cell type manufactured by a process of a volatile semiconductor memory.

In an N-type MOS transistor MN2 functioning as the operation enabler MN2, a drain is connected to a connection node NO1, and a source is grounded. If a state of an enable signal EN, which can be provided as a mode register set(MRS) code, is "H", the N-type MOS transistor MN2 is turned on, to connect a source of the MOSFET MN1 of the EEPROM cell type to a ground power. The NMOS transistor MN2 is turned on by the enable signal EN that is applied as "H" only in program and erase operating modes.

The latch L1 latches, as the status information, a voltage level appearing in the source of the MOSFET MN1 according to a change of threshold voltage of the MOSFET MN1, in case a defect address is stored.

To reduce a current consumption in a read operation, the fuse device MN1 shown in FIG. 2 functions as an on-cell only

in case the fuse device MN1 should store the defect address. Thus, initially, a plurality of fuse devices are all programmed and provided as an off-cell state. Under such a state, only fuse devices for storing the defect addresses are selectively erased and become an on-cell state. That is, the transistor MN1 having a threshold voltage increased through a program operation operates as an off-cell in the read operation, and the transistor MN1 having a threshold voltage lowered through the selective erase operation operates as an on-cell in the read operation.

For example, if the transistor MN1 of FIG. 2 is an erased cell transistor, the transistor MN1 functions as the on-cell in the read operation and a logic level "H" is provided in the node NO1. Thus, a logic level of a redundancy enable signal PREi of an inverter IN3 for inverting an output of the latch L1 is outputted as "H". Therefore, a corresponding normal memory cell is replaced with a redundancy memory cell.

In the meanwhile, if the transistor MN1 of FIG. 2 is a programmed cell transistor, the transistor MN1 functions as the off-cell in the read operation and a logic level "L" is provided in the node NO1, thus a logic level of the redundancy enable signal PREi of the inverter IN3 is outputted as "L". That is, a corresponding normal memory cell performs an original cell function without a replacement by the redundancy

memory cell.

Consequently, if an error bit for a memory is changed with a connection circuit, the circuit of FIG. 2 functions as a defect address storage circuit for latching an address of the error bit by a conductive or non-conductive control of the fuse device MN1, and the fuse device MN1 employs a non-volatile memory device manufactured in a volatile semiconductor memory fabrication environment.

Though the fuse device of FIG. 2 was above described as an example for the case used within the defect address storage circuit; in case a mode entry signal indicating an entry to a specific operating mode such as a test mode etc. is stored, it can be, of course, used as the fuse device.

Further, if the MOSFET MN1 of the single polysilicon EEPROM cell type is erased by a working fault, the transistor MN1 is restored to an off-cell once a program was re-executed, which is also efficient when again restoring to an original condition after performing the test.

Next, the fuse device of FIG. 2, namely, the MOSFET MN1 of the single polysilicon EEPROM cell type will be described on a structure etc. as an example without limiting the invention.

FIG. 3 illustrates a layout of the fuse device referred to FIG. 2 and FIG. 4 is a sectional view of an X-X' line shown in FIG. 3. Referring to FIGS. 3 and 4, a first conductive

substrate 10 is formed as a P-type semiconductor substrate made of single-crystal silicon. A second conductive deep well 20 is formed on one portion of the first conductive substrate 10 through an ion implantation process of selectively ion-implanting an n-type impurity. In the second conductive deep well 20, a first conductive pocket well 40 is formed through an ion-implantation process of injecting a p-type ion. Source 50 and drain 60 are formed by injecting an n+ type ion into a portion of the p-type pocket well 40. While, a second conductive well 30 is spaced from the second conductive deep well 20, and is formed on another portion of the first conductive substrate 10. A second conductive ion-implantation region N+ formed on a portion of the second conductive well 30 functions as a control gate 80. Because the control gate 80 is formed within the n-well 30, it is no need to specifically form a polysilicon film on an upper part of the floating gate. Thus, a structure of the single polysilicon EEPROM cell type in which only the floating gate is formed with a polysilicon film, can be realized. On an upper part of a channel region as a boundary region between the source 50 and the drain 60, and on partial upper parts of the first conductive pocket well 40, the second conductive deep well 20, the substrate 10, the second conductive well 30 and the control gate 80; a tunnel oxide film 65 having a thickness of about 70Å through 100Å, and a charge storage floating gate 70 are formed in length.

That is, the floating gate 70 is formed extendedly till a partial upper part of the control gate 80, passing on upper parts of the first conductive pocket well 40 and the second conductive deep well 20, in a direction roughly right-angled to the source-drain channel. The floating gate 70 is made of polysilicon layer material deposited through a chemical vapor deposition, and functions as a charge storage floating gate of EEPROM cell type. The floating gate 70 is formed as a single layer on an upper part of the tunnel oxide film 65, and can be made simultaneously when a gate of a transistor is manufactured in a DRAM fabrication process. Though the source 50 and the drain 60, and the control gate 80 were formed under the floating gate 70 as shown in the drawing, they are actually manufactured through an ion-implantation and a diffusion process after fabricating the floating gate 70.

In the exemplary embodiment of the invention, the MOSFET MN1 of the single polysilicon EEPROM cell type having such a structure is manufactured by a process of a volatile semiconductor memory such as a DRAM etc., and is used as a fuse device for storing status information.

An operation of the fuse device MN1 having such a configuration has program and erase and read operating modes same as the EEPROM memory cell transistor, while the fuse device MN1 is different only for a voltage apply condition therefrom.

First, the program operation is performed by applying a voltage over 5volt to the control gate, a ground voltage to a source terminal, and a voltage over 3volt to a drain terminal. Once the voltage is applied, hot electron generated in a channel formed on a silicon interface contacted with a gate oxide film is injected into the floating gate 70. Once a negative(-) charge is sufficiently accumulated in the floating gate 70, a threshold voltage of the memory cell transistor MN1 rises more than a threshold voltage provided before a programming and the memory cell transistor MN1 thus functions as an off-cell. The threshold voltage of the programmed memory cell transistor MN1 has a voltage distribution of about 4V-6V.

Next, the erase operation is performed by applying a ground voltage to the control gate, and a voltage over 5volt to the source terminal or the drain terminal. Herewith, one terminal among the source and drain terminals, to which the voltage is not applied, becomes a floating state. When the voltage is applied, electron injected into the floating gate is discharged through a Fowler-Nordheim(F-N) tunneling method, thus a changed threshold voltage returns to an original peculiar threshold voltage. When the F-N tunneling occurs, a negative(-) charge captured within the floating gate 70 is discharged to the source or drain. It is generally known that the F-N tunneling occurs when electric field of 6-7 MV/cm interposing an isolation film is applied to a conductive layer.

In the memory cell transistor, the tunnel oxide film 65 is formed with thickness of about 80Å, thus the F-N tunneling can occur.

Further, the read operation is performed by applying 2V through 2.5V to the drain and the control gate of the memory cell transistor under such a state that the source region floats. In the read operation, the memory cell transistor having a threshold voltage increased by the program operation operates as an off-cell to thus cut off a flowing of current from the drain to the source. In this case the memory cell transistor operates as the "off-cell".

During the read operation, a memory cell having a threshold voltage lowered by the erase operation has a current path formed from a drain region to a source region, and operates as an on-cell. In this case the memory cell transistor is called an "on-cell". The threshold voltage of the erased memory cell transistors generally has a voltage distribution of about 1V through 2V.

The operating modes based on the voltage apply conditions are arranged as shown in the following table 1.

[Table 1]

Operating Mode	IN1 (Control Gate)	VCC (Drain)	S/L (Source)
Program	+5V	+2.5~3V	0V
Erase	0V	+5V	0V, Floating
Read	+2.0~2.5V	+2.5~3V	Floating

As shown in Table 1, the fuse device of the invention

can perform an operation like the memory cell transistor of the EEPROM within an operating voltage range of a volatile semiconductor memory.

As shown in FIGS. 3 and 4, the reason why the field effect transistor having the source 50 and the drain 60 is disposed within the deep n-well 20, is to prevent a short from other elements in the erase operation. In other words, a PN junction is generated between the control gate and the drain terminal receiving a high voltage in the erase operation, and if there is no deep n-well, a short from other elements may be caused in the substrate.

FIG. 5 is a simulation graph illustrating a program operation characteristic of the fuse device referred to FIG. 2. Referring to FIG. 5, a transverse axis indicates a drain voltage and a vertical axis designates a drain current, and the graph provides a case that an N-type MOS transistor having a channel length of 0.6μm is manufactured through a CMOS fabrication process having an LDD structure. Herewith, it results in that a coupling ratio of the N-type MOS transistor functioning as the fuse device has about 0.7~0.8 and that the program operation is performed at a region where a drain voltage is 3V in case a voltage applied to the control gate is about 5V. Also, if a channel length is more reduced, a program apply voltage can be lowered more.

As described above, the inventive fuse device is

electrically cut without breakage caused by using laser beam or current. In addition, an operation like a memory cell transistor of EEPROM can be performed within an operation voltage range of a volatile semiconductor memory.

It will be apparent to those skilled in the art that modifications and variations can be made in the present invention without deviating from the spirit or scope of the invention. Thus, it is intended that the present invention cover any such modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents. For instance, transistor devices employed in the circuit can be varied to an opposite type thereto or a connection construction of the circuit can be varied diversely. Accordingly, these and other changes and modifications are seen to be within the true spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, characterized in that a MOS field effect transistor (MOSFET) of a single polysilicon EEPROM cell type fabricated by a process of a volatile semiconductor memory is used as a fuse device for storing state information.

2. The device as claimed in 1, wherein the single polysilicon of the MOSFET corresponds to a charge storage floating gate of the EEPROM cell, and a control gate of the EEPROM cell corresponds to a second conductive ion-implantation region which is spaced from a channel region of the MOSFET and which is formed under the single polysilicon.

3. The device as claimed in 2, wherein the MOSFET is an n-channel MOSFET, and a program operation for electrically cutting the fuse device is performed by injecting electron into the floating gate through a hot electron injection method.

4. The device as claimed in 3, wherein an erase operation for electrically connecting the fuse device is performed by discharging the electron captured by the floating gate through an F-N(Fowler-Nordheim) tunneling method.

5. A semiconductor integrated circuit device, comprising a defect address storage circuit that has, as a fuse device, a non-volatile memory cell transistor fabricated by a process of a volatile semiconductor memory.

6. A volatile semiconductor memory device, which has a plurality of volatile memory cells, and a defect relief circuit for controlling an electric connection or cut-off of a fuse device to replace a defect memory cell out of the volatile memory cells by a redundancy memory cell, said device characterized in that:

the defect relief circuit employs a MOSFET of a single polysilicon EEPROM cell type as the fuse device, said MOSFET being changed from a first threshold voltage level to a second threshold voltage level in response to an applied program control signal, and being changed from the second threshold voltage level to the first threshold voltage level in response to an applied erase control signal, whereby resulting in an electric cutting and connection of the fuse device without a breakage.

7. A defect address storage circuit of a semiconductor integrated circuit device, said circuit comprising:

a MOSFET of a single polysilicon EEPROM cell type, in which a drain is connected to a first power source and a

control gate is connected to a second power source, to function as a fuse device for storing status information, and which is manufactured by a process of a volatile semiconductor memory;

an operation enabler for connecting a source of the MOSFET to a ground power in response to a status of an enable signal; and

a latch for latching, as the status information, a voltage level appearing in the source of the MOSFET according to a change of the threshold voltage of the MOSFET, in storing a defect address.

8. The circuit as claimed in 7, wherein the source of the MOSFET is grounded and the first and second power sources are each about 3 volt and 5 volt, in a program operation.

9. The circuit as claimed in 8, wherein the source of the MOSFET is grounded or floats, and the first and second power sources are each about 5 volt and 0 volt, in an erase operation.

10. The circuit as claimed in 9, wherein the source of the MOSFET floats and all the first and second power sources are about 3 volt, in a read operation.

11. The circuit as claimed in 7, wherein the operation enabler is an N-type MOS transistor.

12. The circuit as claimed in 7, wherein the latch is an inverter latch in which input terminals are connected with output terminals one another.

13. The circuit as claimed in 7, further comprising an output inverter for inverting and outputting an output of the latch.

14. A dynamic random access memory comprising:

a MOSFET of a single polysilicon EEPROM cell type, which is manufactured by a process of a volatile semiconductor memory, to be used as a fuse device for storing status information, said MOSFET including,

a first conductive substrate;

a second conductive deep well formed on one portion of the first conductive substrate;

a first conductive pocket well formed within the second conductive deep well;

source and drain formed as a second conductive ion-implantation region in a portion of the first conductive pocket well;

a second conductive well formed on another portion of

the first conductive substrate, being spaced from the second conductive deep well;

a control gate formed as a second conductive ion-implantation region in a portion of the second conductive well; and

a floating gate of polysilicon layer material extendedly formed till a partial upper part of the control gate, passing through upper parts of the first conductive pocket well and the second conductive deep well in a direction roughly right-angled to the source-drain channel, and interposing a tunnel oxide therebetween.

15. The memory as claimed in 14, wherein the second conductive type is an n-type impurity if the first conductive type is a p-type impurity.

FIG.1 (PRIOR ART)

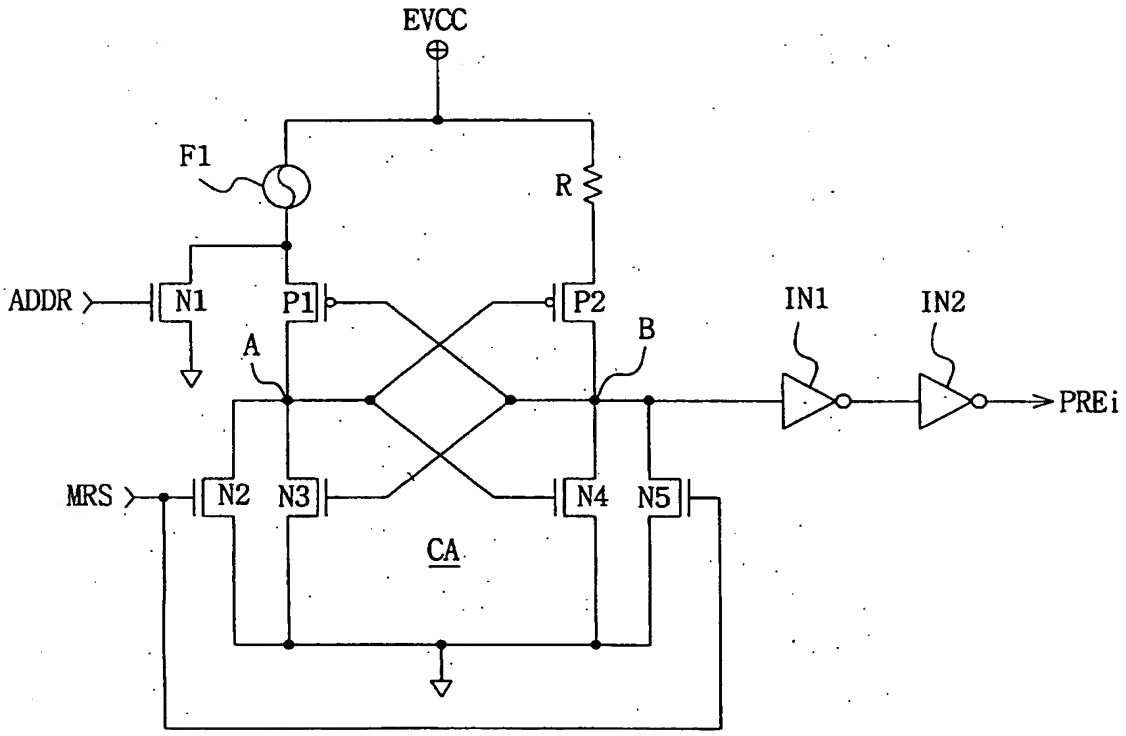


FIG.2

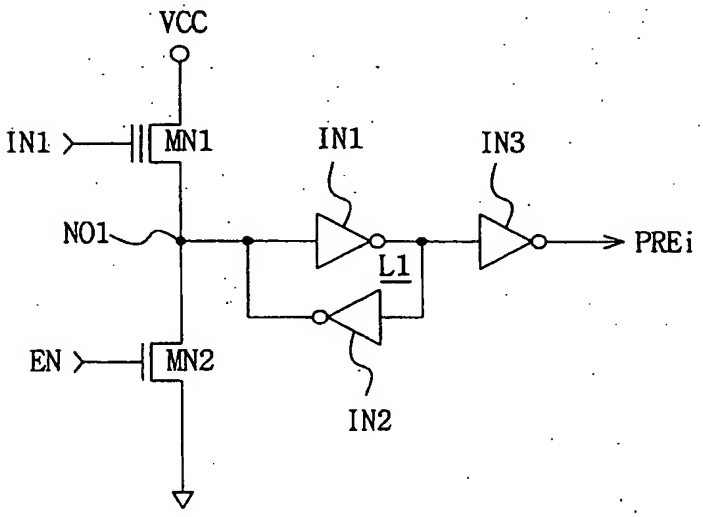


FIG.3

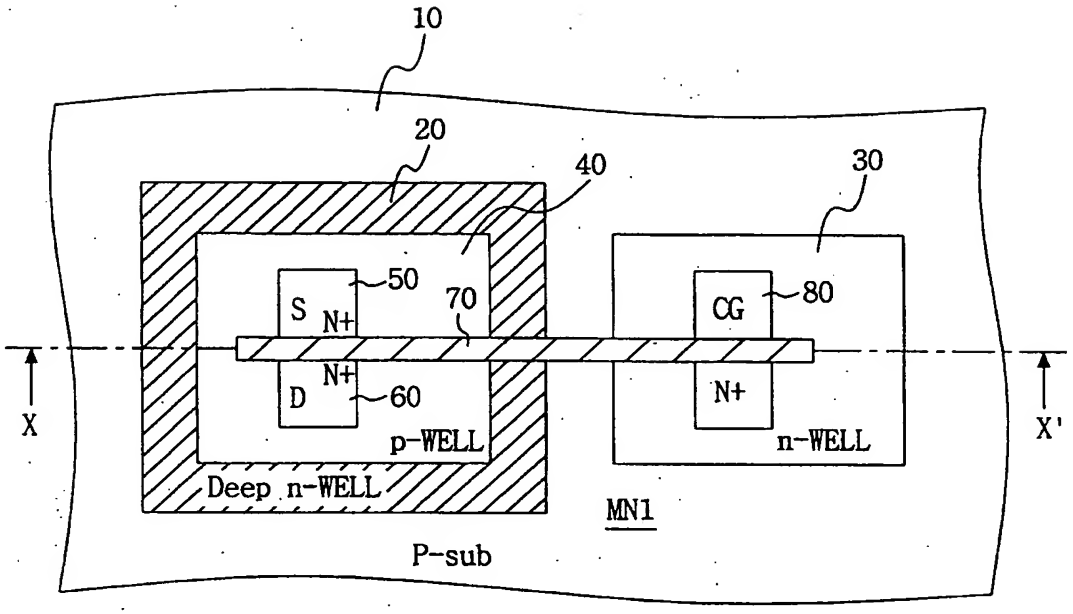

10
20
40
30
50
S
N+
70
CG
80
N+
D
60
N+
X
X'
p-WELL
n-WELL
Deep n-WELL
MN1
P-sub

FIG.4

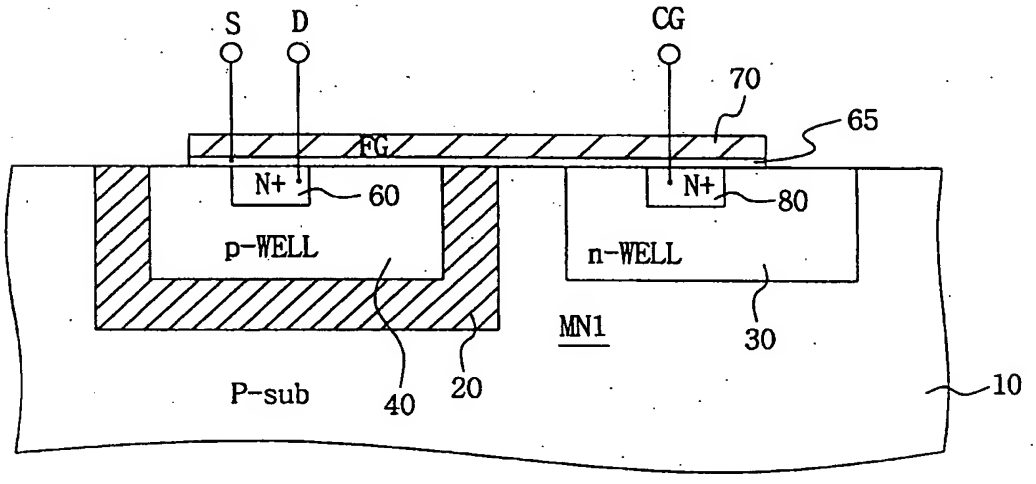
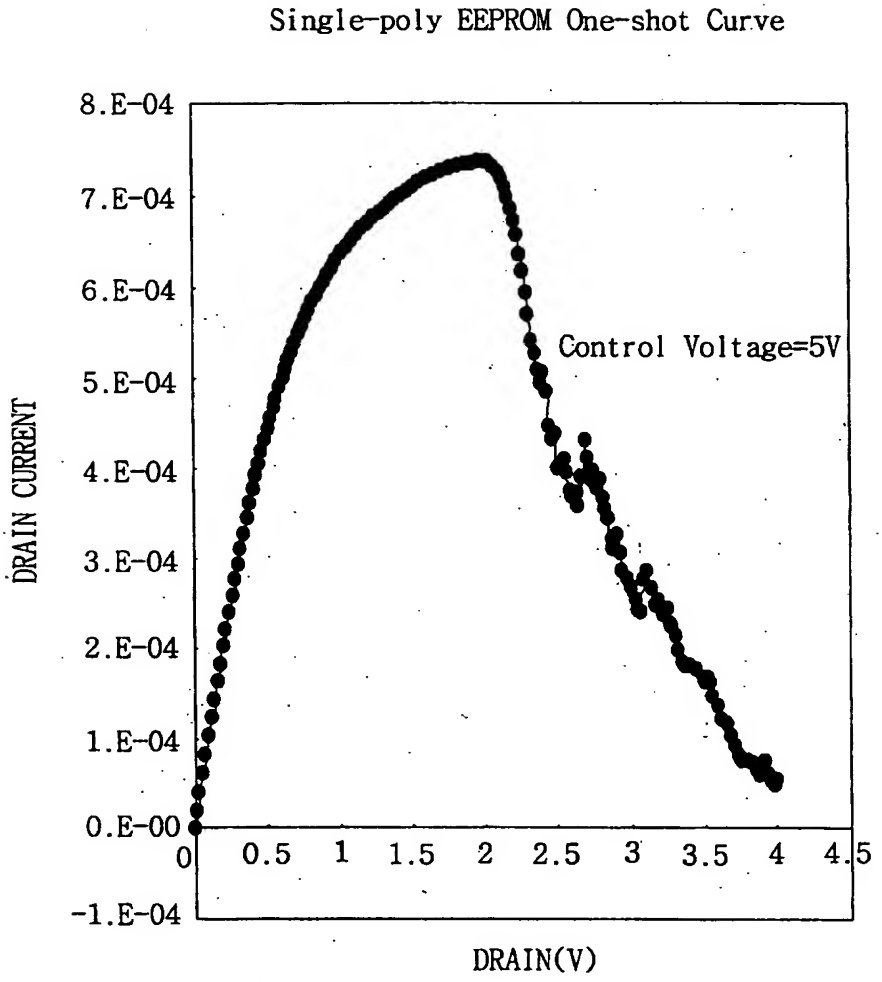

S
D
CG
70
65
FG
N+
60
N+
80
p-WELL
n-WELL
MN1
30
P-sub
40
20
10

FIG.5


Single-poly EEPROM One-shot Curve
8.E-04
7.E-04
6.E-04
5.E-04
4.E-04
3.E-04
2.E-04
1.E-04
0.E-00
-1.E-04
DRAIN CURRENT
Control Voltage=5V
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
DRAIN(V)